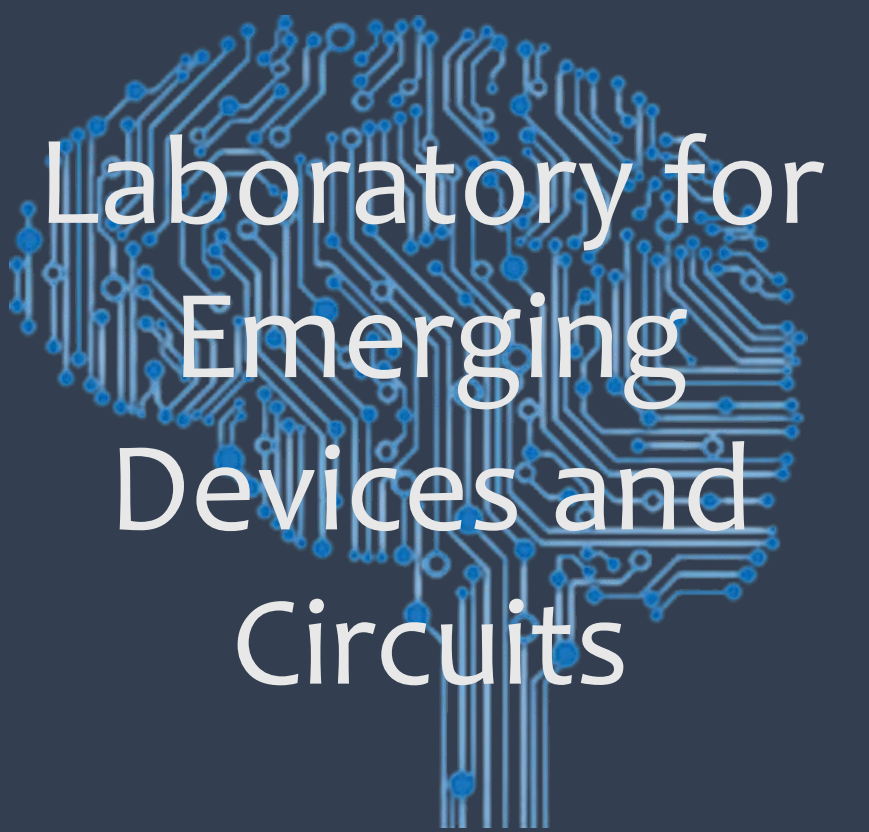




# OPERATION VOLTAGE IMPACT AND WORKLOAD MODELING OF NBT/PBTI IN OXIDE DEVICES



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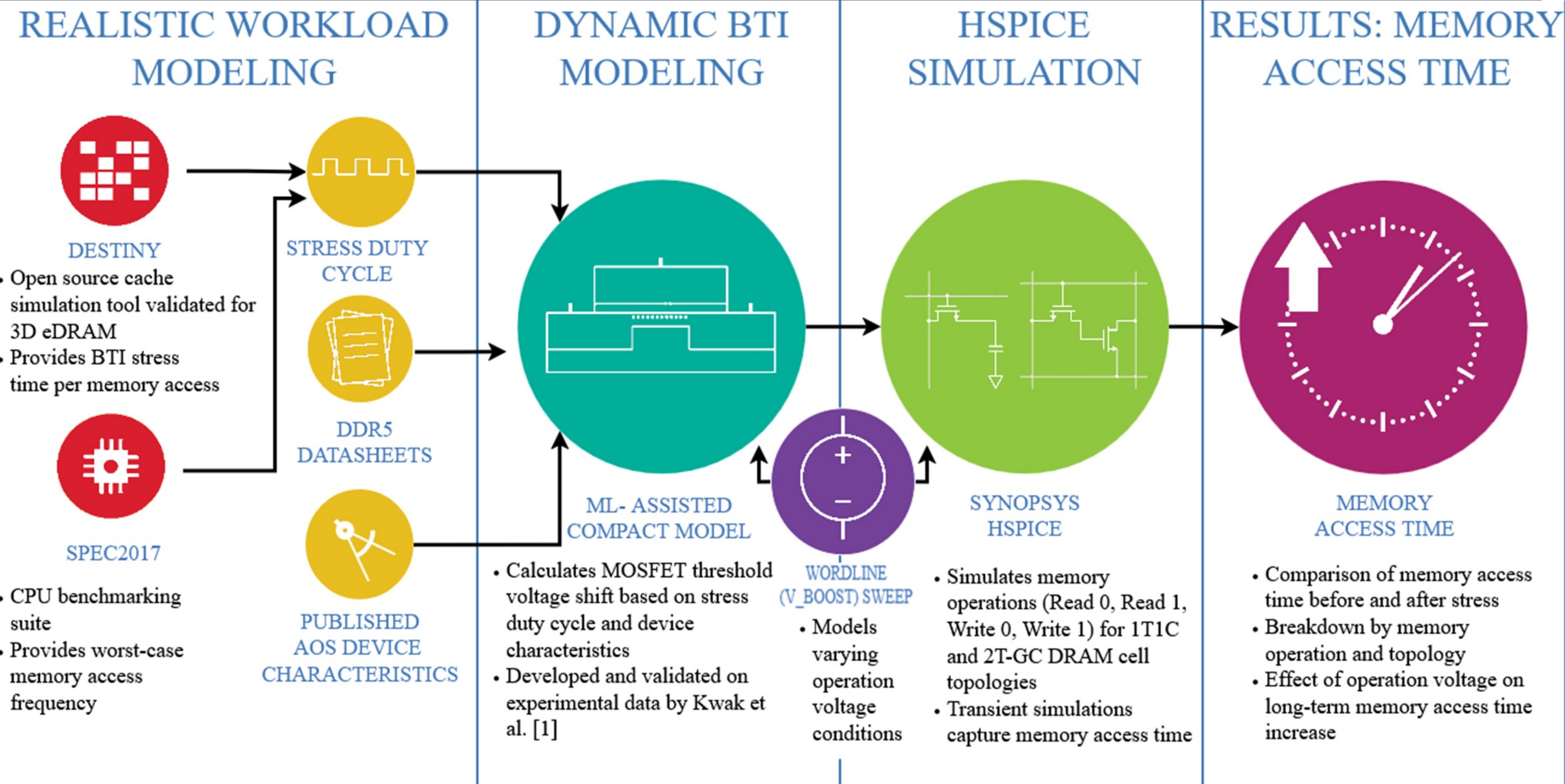
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## Introduction

- Memory is the bottleneck of modern, high-performance computing.
- Advances in processing power have caused memory bandwidth to fall behind, creating a **memory wall**. New solutions are needed at the **device** and **material levels**.
- Amorphous Oxide Semiconductors (AOS)**
  - Emerging class of materials with **low leakage current** & **low deposition temperatures**
  - Compatible with **Monolithic 3D Integration**—memory stacked atop logic layers on the back end of line (BEOL)—**greatly improving interconnect density & bandwidth**
- AOS-based Dynamic Random Access Memory (DRAM) faces reliability issues impacting performance:**
  - Bias Temperature Instability
  - Large transition region ( $V_{TR}$ ): a difference between the voltage of the subthreshold (off) and above threshold (on) states

## Simulation Framework



## Conclusion

- BTI Performance Modeling**
- Substantial increases in access time were observed across all operations and topologies following BTI stress
  - 2T-GC is more resistant to BTI-induced access time increases for write operations
  - Decreases in wordline voltage **strongly correlate** to reductions in long-term access time increases
- VTR Characterization**
- Vertical & Channel-All-Around (CAA) FET structures exhibit lowest  $V_{TR}$  and **provide greatest opportunity for  $V_{OV}$  reduction.**

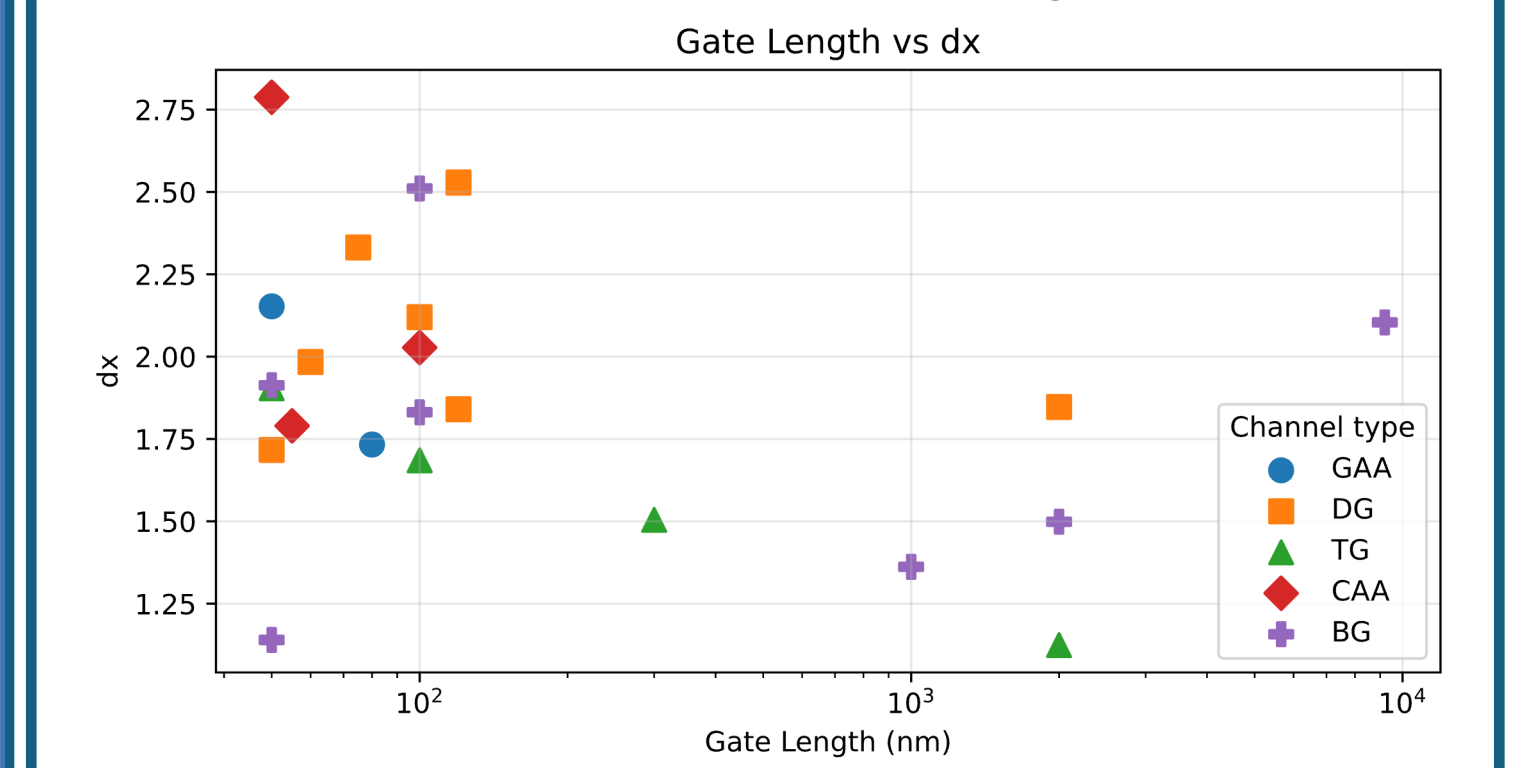


Fig. 5. Deviation of subthreshold swing for varying gate lengths and channel types.

## Objective #1: Bias Temperature Instability Performance Modeling

- BTI: Key reliability concern in MOSFETs**
- Symptom: Shift in threshold voltage ( $V_{TH}$ ) over time
- Effects: Reduced current & higher access time

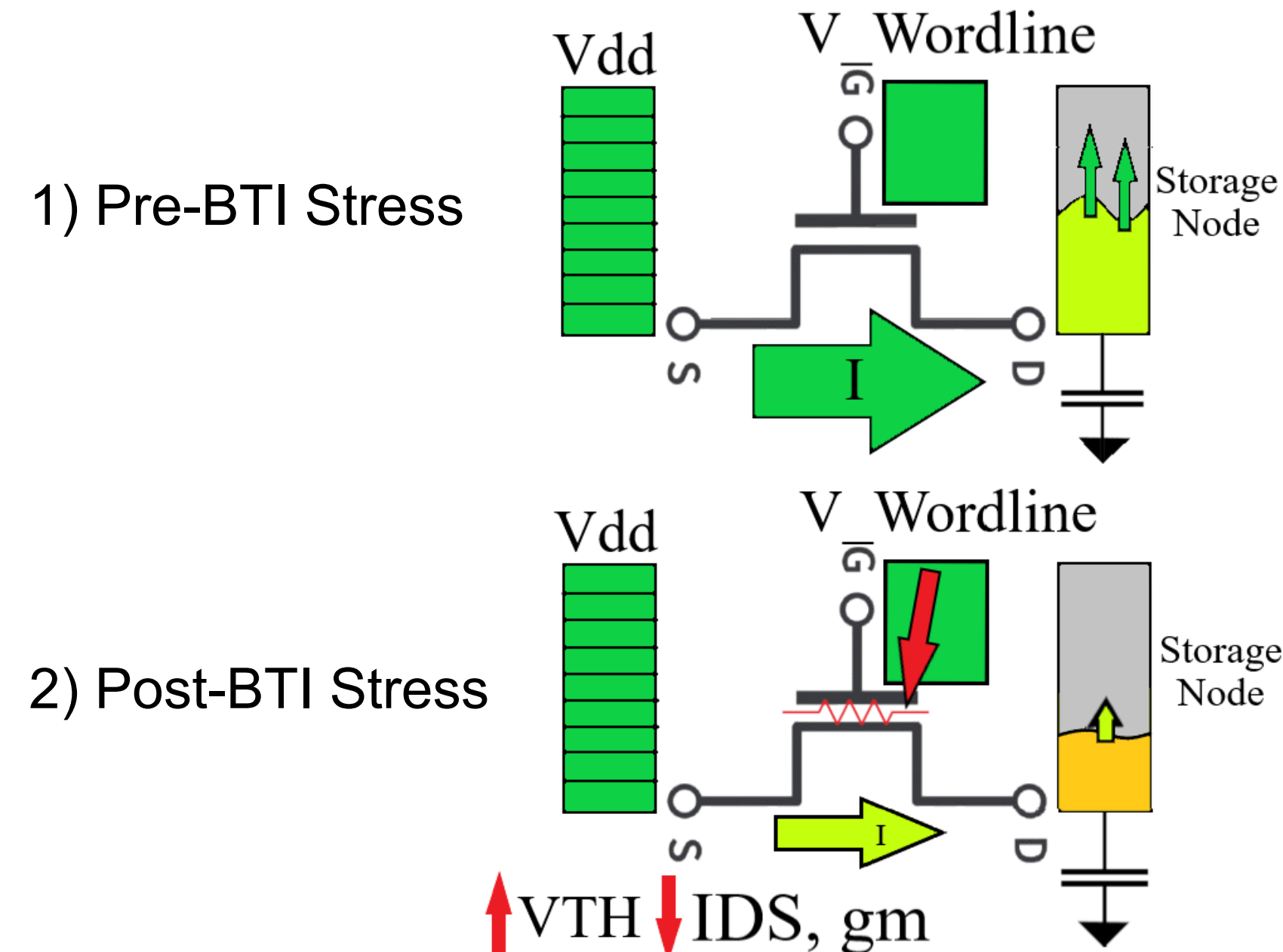


Fig. 1. BTI effect on DRAM write 1 operation.

**How Does Wordline Voltage Affect Long-term Latency Increase Due to BTI Effects?**

## Objective #2: VTR Characterization & Literature Survey

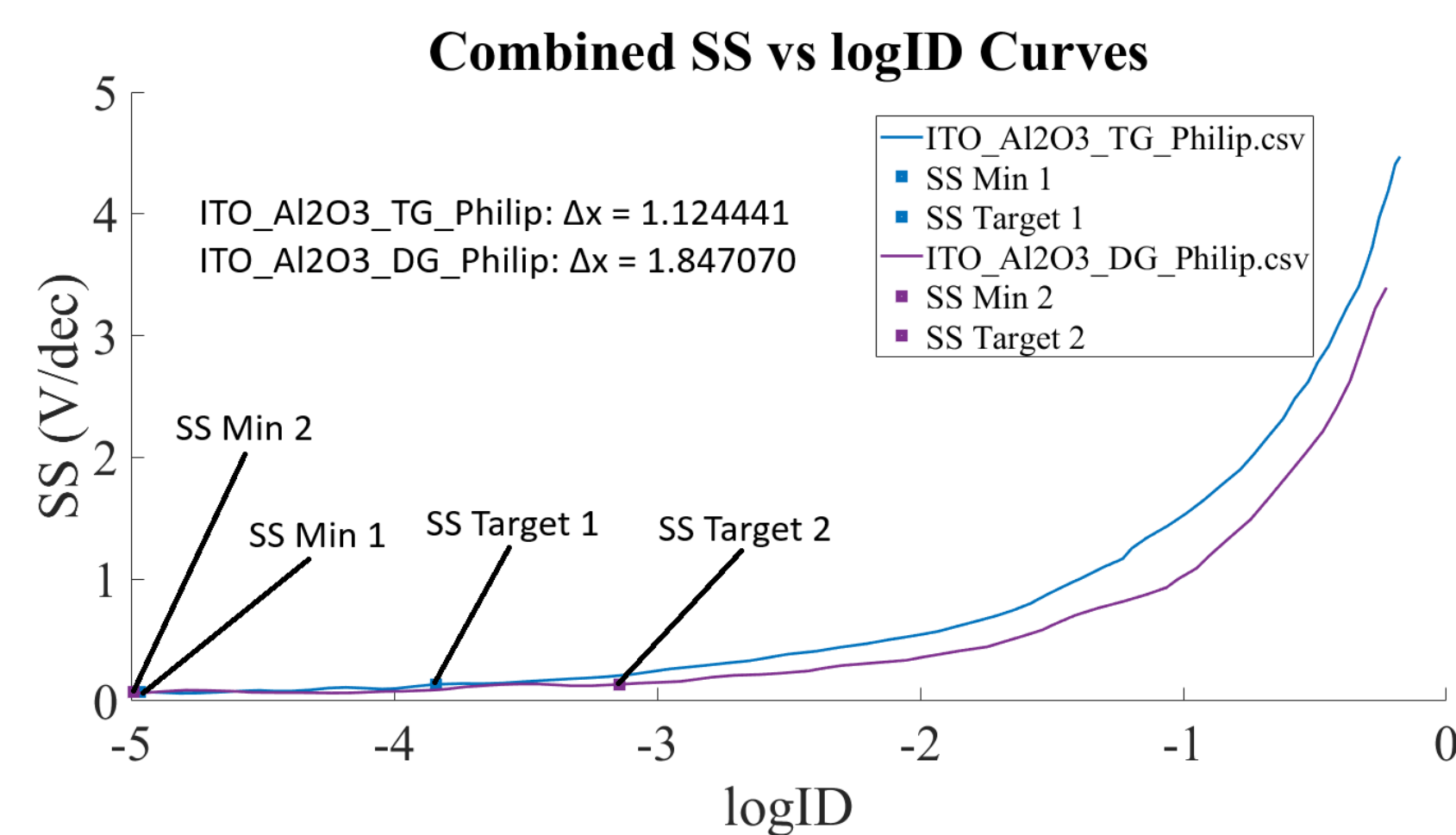


Fig. 2. Visualization of VTR characterization process.

- Jana et al. proposed that later deviation (greater  $\Delta x$ ) of subthreshold swing (SS) over  $\log_{10}(I_D)$  curve  $\rightarrow$  smaller  $V_{TR}$  [2]

$$1) SS_{min} = \frac{1}{10} \sum_{i=1}^{10} \overline{SS}_i \quad 3) \Delta x = \overline{x}_{target} - \overline{x}_{min}$$

$$2) |\overline{SS}_{target} - \overline{SS}_{min}| = 0.75 |\overline{SS}_{min}|$$

**Which MOSFET Structures Feature Lower  $V_{TR}$  that Enable Reductions in  $V_{TH}$  and  $V_{WORDLINE}$ ?**

## Results

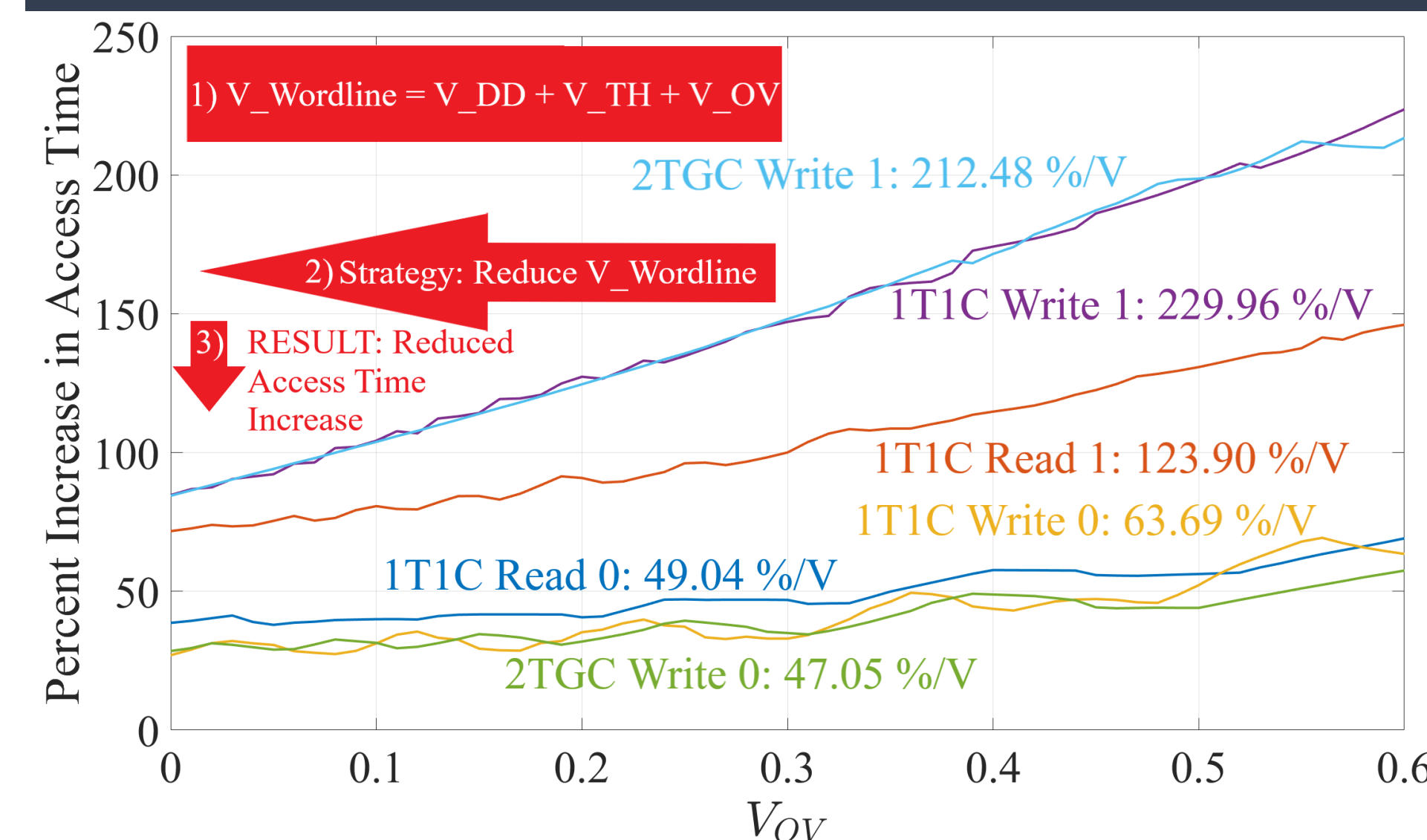


Fig. 3. Increase in access time following 1000 seconds of simulated stress at varying wordline voltages for each operation and topology. Average access time increases per volt are labeled.

Average $V_{TR}$ Characterization Values in $\log_{10}(I_{DS})$						
MOSFET Structures (AOS)		Gate Structures (AOS)			Silicon Baseline	
Planar	Vertical	GAA	CAA	Dual Gate	Back Gate	Top Gate
1.798	1.944	1.688	2.202	2.052	1.766	1.514
						3.385

Fig. 4. Literature review results of 19 works on AOS devices showing  $V_{TR}$  characterizations of different MOSFET and gate structures.

- Significance**
- We demonstrate a simulation-based framework for modeling BTI-induced increases in access time in AOS-based DRAM under **realistic workloads**
  - Wordline voltage reductions are shown to be an **effective method of mitigating BTI effects** when combined with reductions of  $V_{TR}$  and  $V_{TH}$  through **careful selection of MOSFET and gate structures.**

## References

[1] J. Kwak, S. Deng, C. Zhang, G. Jeong, O. Phadke, S. G. Kirtania, J. Lee, S. Datta, and S. Yu, "Machine learning-assisted compact modeling of ac stress-induced bias temperature instability in top- and bottom-gate w-doped in channel semiconductor transistors," IEEE Transactions on Electron Devices, vol. 72, no. 8, pp. 4163–4169, 2025

[2] K. Jana, J. Kang, S. Liu, F. F. Athena, C.-H. Huang, Y. Tang, H. J.-Y. Chen, B. Saini, J. Hartanto, R. K. A. Bennett, A. O. E. Persson, S. Li, K. Neilson, Y.-M. Lee, K. Leitherer, K. Nomura, P. C. McIntyre, E. Pop, and H.-S. P. Wong, "Key to low supply voltage: Transition region of oxide semiconductor transistors," 2025 Symposium on VLSI Technology and Circuits Digest of Technical Papers, pp. 1–3, 2025.



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