Faaiq Waqar

319 10th St NW, Atlanta, GA 30318

Google Scholar faaiq.waqar@gmail.com linkedin.com/in/faaiqwaqar github.com/faaiqgwaqar

Education

Georgia Institute of Technology **2023 – 2028**

Ph.D. Electrical & Computer Engineering, Minor Physics, Education *GPA: 4.0*

Oregon State University **2017 – 2022**

B.S Computer Science, B.S Electrical & Computer Engineering, Minor Mathematics

Relevant Coursework

- VLSI & Analog Circuits
- Microcontroller Design
- Quantum Mechanics
- Computer Architecture
- Condensed-Matter
- Numerical Methods
- Integrated Photonics
- Theory of Computation

Research Experience

Georgia Institute of Technology, Emerging Devices and Circuits Lab **August 2023 – Present**

Graduate Researcher - Advised by Dr. Shimeng Yu *Atlanta, GA*

- Leading the development of simulation for the modeling and metrology of emerging non-volatile and persistent memories (e.g. MRAM, eDRAM, FeRAM) in high-performance, reconfigurable and mixed-signal neuromorphic computing systems. Leading collaboration efforts in circuit & device simulation with over 7 universities, companies, and research-centers.
- Establishing cross-layer design of emerging ferroelectric, and M3D SRAM based FPGA architectures with fine-grain time-multiplexing using BEOL-compatible FPGA configuration memories from theory (i.e. Xilinx & SPICE simulation, GDS generation) to tapeout (i.e. MUSE TSMC 40nm, 7nm, Global Foundries 28nm HKMG, MIT Lincoln Lab 90nm).
- Extensive experience modeling amorphous oxide semiconductor (AOS) and ferroelectric FETs for memory and low-power logic (negative capacitance) applications through mixed-mode physics simulation, the development of SPICE (i.e. BSIM, Machine Learning assisted) compact models, and logical effort modeling of banked memories timing/energy.
- Actively investigating heterogeneous integration system design through monolothic 3D & heterogeneous 2.5D/3D packaging techniques using EM simulation and analytical modeling of emerging bond and interposer materials.
- Driving collaboration and mentorship in FPGA BRAM design, monolithic 3D DRAM simulation, PIM-centric transposable cache design, and AOS/ferroelectric transistor reliability resulting in 9 co-authored papers

Oregon State University, Simon Ensemble Lab **June 2020 – March 2023**

Undergraduate Research Assistant - Co-Advised by Dr. Xiaoli Fern, Dr. Cory Simon *Corvallis, OR*

- Applied machine learning and mathematical modeling techniques to predict and analyze nano-porous materials (NPMs), accelerating their discovery and deployment in applications such as gas storage, separation, and sensing.
- Led development of Graph Neural Networks (GNNs) for multitask prediction of atom level force-field precursors and molecule level gas uptake in covalent organic frameworks (COFs) using PyTorch/Geometric. Assisted in GNN development for graph level low-pressure CO_2 uptake prediction in metal organic frameworks (MOFs).
- Spearheaded project on the pedagogical use of Bayesian statistical inversion theory for solving and quantifying uncertainty of inverse problems. Section of work now used for CHE361 - Chemical Process Dynamics and Simulation.
- Implemented Julia package for conversion of Crystalline Information (.cif/.xyz format) to usable graph representation and targets in NumPy (.np) and PyTorch (.pt) formats. Used in translation of 50,000+ NPMs on various projects.

Work Experience

TSMC **May 2026 – August 2026**

Incoming Corporate Research Intern *San Jose, CA*

Microsoft **July 2022 – August 2023**

Hardware Engineer *Hillsboro, OR*

- Design and development of performance, debug and test systems for first generation custom Microsoft Azure SoCs
- Microarchitected and implemented (RTL, RTL2PD) custom IPs used for test and debug infrastructure.
- Owner of multiple DFD subsystems including performance monitors and CoreSight infrastructure used for silicon bringup. Managed system level integration, architecture, power-gating/clock-gating and timing analysis and optimization, repo/release management, SRAM, Fuse & ROM integration, documentation etc.
- Supported implementation of DFD subsystems across SoC through expertise on device operation and implementation.
- Wrote tool flows and architecture specification documentation for larger hardware engineering organization.

Arm **June 2021 – September 2021**

CPU Engineering Intern *Austin, TX*

- Enhanced tools for system level testing of Armv8 & Armv9 cores applied by validation engineers. Utilized and expanded the BURST (orig. ProValid) tool on FPGAs, emulation, simulation (RTL), & silicon (Neoverse N1 MicroArchitecture).
- Implemented flow for integration of 5+ FPGA images and 4 Silicon platforms on BURST continuous integration. Wrote Ruby/Shell scripts to upload dstream, compile binaries, lock platforms, connect UART etc. autonomously.
- Modularized the collection and interpretation of performance data collected on BURST across platforms using Python.
- Designed & implemented parsing automation flow to collect cycle tag data and load into the company database.

Oregon State University **May 2018 – June 2022**

Various Roles: Teaching Assistant, Tutor, Software Developer, Database Admin *Corvallis, OR*

- Leading labs, delivering recitation lectures, grading and holding office hours for ENGR 201 and ENGR 202 (Electrical Fundamentals I & II), focused on subject matter of AC/DC circuit analysis.
- Assisting undergraduate students through private/group sessions to guide them in succeeding in coursework in Electrical & Computer Engineering, Mathematics, and Computer Science.
- Implemented large scale ASP.NET, C# API solutions for ODEQ Clean Fuels Program, used to report transportation fuels & emissions in Oregon. Development in SCRUM iterations with sprints tracked in Azure DevOps.
- Lead FB360 Database for more than seven years of event data (attendance, business mapping, trend data on advisor topics, and translating into visualization data for 6000+ data points improving future market events).

Intel **Nov 2016 – February 2017**

Client Computing Group Intern *Hillsboro, OR*

- Using CRM software, managed organization's premiere support services for large account error details including Comcast. Reported on change logs into Jira and Salesforce. Visualization of routine procedures by tracking IPS.

Technical Skills

Programming Languages: C, C++, Python, System Verilog, Julia, Matlab, Javascript, Assembly, Ruby
EDA Tools: [Synopsys] (Questa CDC, RDC, VCLP, Verdi), Verilog-to-Routing (VTR), [ARM] Memory Compiler, [NVIDIA] NVBit, ModelSim, Quartus, Fusion, Eagle
Hardware & IP: Xilinx FPGAs, AVR, [Arm] (AMBA, CoreSight), ATMega, PCIe, JTAG, SPI, UART,
Simulation: [Cadence] Virtuoso, [Synopsys] (HSPICE, TCAD), Accel-Sim, GEM5, HSpice, Ramulator, NeuroSim
Machine Learning: PyTorch, PyTorch Geometric, TensorFlow
Databases: Node.js, MongoDB, SQL

Accepted Publications & Proceedings

1. **F. Waqar**, M. Chen, Z. He, Z. Wan, M. Shon, W. Huang, J. Cong, S. Yu, "Enabling Context-Switchable Monolithic 3D FPGA Design Using Bistable Ferroelectric Inverters," IEEE International Sumposium On Field-Programmable Custom Computing Machines (FCCM), 2026.

2. H. Lee*, **F. Waqar***, H. Park, C. Zhang, J. Shin, E. Sarkar, H. Kim, C. Im, M. Hong, D. Ha, A. Khan, S. Yu, S. Datta "Workload-Derived AC Bias Temperature Instability and Mechanism Contributions in BEOL Oxide Channel DRAM Access Transistors," IEEE/JSAP Symposium on VLSI Technology and Circuits (VLSI), 2026.

3. **F. Waqar**, J. Zhang, A. Lu, Z. He, J. Cong, S. Yu, "Monolithic 3D FPGA Design and Synthesis Using Back-End-of-Line Configuration Memories," IEEE/ACM Design Automation Conference (DAC), 2025.

4. **F. Waqar**, J. Kwak, J. Lee, M. Shon, M. Gholamrezaei, K. Skadron, S. Yu, "Optimization and Benchmarking of Monolithically Stackable Gain Cell Memory for Last-Level Cache," IEEE Transactions on Computers (T-Computer), 2025.

5. **F. Waqar**, M.Y. Lee, S. Yoon, S. Lim, S. Yu, "CMOS+X: Stacking Persistent Embedded Memories based on Oxide Transistors upon GPGPU Platforms," IEEE/ACM International Symposium on Memory Systems (MEMSYS), 2025.

6. S. Deng*, J. Sonawane*, **F. Waqar***, O. Phadke*, C. Zhang, M.Y. Lee, S. Yu, S. Datta, "Demonstration of 3T0C with Self-Aligned Oxide Transistors for Parasitic-Aware Design at Array-level," IEEE International Electron Devices Meeting (IEDM), 2025. *Equal Contribution

7. **F. Waqar**, S. Patel and C. Simon, "A tutorial on the Bayesian statistical approach to inverse problems," APL Machine Learning, 2023. DOI

8. Y. Kong, J. Jia, A. Lu, **F. Waqar**, Y.C. Luo, H. Li, I. Young, S. Yu "Digital Compute-in-Memory Ising Annealer with Ferroelectric Capacitor-Based nvSRAM for Combinatorial Optimization Problems," IEEE International Symposium on Circuits and Systems (ISCAS), 2025.

9. J. Lee*, M. Shon*, **F. Waqar**, S. Yu "3-D Digital Compute-in-Memory Benchmark with A5 CFET Technology: An Extension to Lookup-Table-Based Design," IEEE Transactions on VLSI Systems (T-VLSI), 2025. *Equal Contribution

10. S. Kirtania, O. Phadke, E. Sarker, K. Aabrar , D. Chakraborty , **F. Waqar** , J. Shin , T.H. Pantha , S. Dutta, A. Khan , S. Yu, S. Datta, "Amorphous Indium Oxide Channel FeFETs with Write Voltage of 0.9V and Endurance $> 10^{12}$ for Refresh-free 1T-1FeFET embedded Memory," IEEE Transactions on Electron Devices (TED), 2025.

11. S.G. Kirtania, **F. Waqar**, D. Chakraborty, J. Shin, E. Sarkar, J. Reiss, J. Yeager, D. Wolfe, S. Yu, S. Datta "Radiation-Resilient Amorphous Indium Oxide FeFETs for Embedded Nonvolatile Memory," IEEE International Reliability Physics Symposium (IRPS), 2025.

12. E. Sarkar*, C. Zhang*, D. Chakraborty, **F. Waqar**, S. Kirtania, K. Aabrar, H. Park, J. Shin, M. Tian, A. Khan, S. Yu, S. Datta, "First Demonstration of W-doped In_2O_3 Gate-All-Around (GAA) Nanosheet FET with Improved Performance and Record Threshold Voltage Stability," IEEE International Electron Devices Meeting (IEDM), 2024. *Equal Contribution

13. S. Kirtania, O. Phadke, E. Sarker, K. Aabrar , D. Chakraborty , **F. Waqar** , J. Shin , T.H. Pantha , S. Dutta, A. Khan , S. Yu, S. Datta, "Amorphous Indium Oxide Channel FeFETs with Write Voltage of 0.9V and Endurance $> 10^{12}$ for Refresh-free 1T-1FeFET embedded Memory," IEEE International Electron Devices Meeting (IEDM), 2024.

14. W. Huang, J. Jia, Y. Kong, **F. Waqar**, T. Wen, M. Chang, S. Yu, "Hardware Acceleration of Kolmogorov–Arnold Network (KAN) for Lightweight Edge Inference," Asia and South Pacific Design Automation Conference (ASP-DAC), 2024. DOI

15. A. Raza, **F. Waqar**, A. Sturluson, C. Simon, and X. Fern, "Towards explainable message passing networks for predicting carbon dioxide adsorption in metal-organic frameworks," NeurIPS ML4Molecules Workshop, 2020. DOI

Under Review

1. W.H. Huang, J. Jia, Y. Kong, **F. Waqar**, T.H. Wen, M.F. Chang, S. Yu, "Hardware Acceleration of Kolmogorov-Arnold Network (KAN) in Large-Scale Systems," IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), 2025.

2. M.Y. Lee, **F. Waqar**, H. Yang, M.A.U Karim, H. Simka, S. Yu, "Architecting Long-Context LLM Acceleration with Packing-Prefetch Scheduler and Ultra-Large Capacity On-Chip Memories," IEEE MICRO, 2025.

3. J. Kwak, **F. Waqar**, S. Yu, "Monolithic 3D Voltage Converter Enabled Fine-Grain Dynamic Voltage Frequency Scaling in Many Core Processors," IEEE Transactions on Computers (T-Computer), 2025.

4. M. Chen, **F. Waqar**, J. Jia, V. Garg, S. Yu, "A Non-Volatile FPGA Desing with Dual-FeFET Configuration Memory in 28nm Foundry Process," GOMACTech, 2025.

5. J. Kim, D. Baig, **F. Waqar**, S. Yu, M. Bakir, C. Hao, "Omelet: A Technology- and Structure-Aware Interconnect Simulator for 2.5D/3D Chiplet Systems," International Symposium on High Performance Computer Architecture (HPCA), 2026.

Patents

1. S. Yu, **F. Waqar**, M. Chen "Non-Volatile Reconfigurable Switch Design based on Programmable Threshold Voltage Transistors," [Filed], 2026.

2. S. Yu, M. Chen, **F. Waqar**, "Non-Volatile Lookup Table Design based on Programmable Threshold Voltage Transistors," [Filed], 2025.

3. J. Kim, D. Baig, **F. Waqar**, "Technology-Aware Hierarchical Network Interconnect Simulator for 2.5D/3D Chiplet Systems," [Filed], 2025.

Presentations

- 10/2025. [Oral Presentation] Presented "CMOS+ X: Stacking Persistent Embedded Memories based on Oxide Transistors upon GPGPU Platforms." IEEE/ACM International Symposium on Memory Systems (MEMSYS) 2025 - Washington D.C, USA
- 6/2025. [Oral Presentation] Presented "Monolithic 3D FPGA Design and Synthesis with Back-End-of-Line Configuration Memories." IEEE/ACM Design Automation Conference (DAC) 2025 - San Francisco, CA
- 11/2024. [Poster Presentation] Presented "3D-FPGA: Monolithic 3D FPGA Design and Synthesis with Back-End-of-Line Configuration Memories." and "Performance Benchmarking and Optimization of M3D Stackable Gain Cell Memory for Ultra-Large Last-Level Cache." SRC/DARPA Year 2 PRISM Center Review - University of California, San Diego
- 6/2022. [Poster Presentation] Presented "Message Passing Neural Networks to Predict Adsorption Properties of Nanoporous Materials." Project Expo 2022 - Oregon State University
- 5/2022. [Poster Presentation] Presented "Message Passing Neural Networks to Predict Adsorption Properties of Nanoporous Materials." Celebrating Undergraduate Excellence - Oregon State University
- 7/2019. [Poster Presentation] Presented "Sensor System for Real-Time Environmental Data Gathering," Summer Undergraduate Research Symposium - Oregon State University

Awards & Fellowships

- 10/2025. Awarded "Best Presentation" - IEEE/ACM International Symposium on Memory Systems
- 3/2025. Awarded "STEER Fellowship" - Georgia Institute of Technology
- 9/2024. Awarded "CREATION Award" - Georgia Institute of Technology
- 8/2023. Awarded "President's Fellowship" - Georgia Institute of Technology
- 4/2023. Awarded "NSF Graduate Research Fellowship" - National Science Foundation
- 11/2021. Awarded "Undergraduate Research Fellow" Notation - Oregon State University
- 1/2019. Awarded "URSA Engage Award." - Oregon State University

Reviewer Service

Conferences: IEEE International Symposium on Workload Characterization (IISWC)
Journals: IEEE Electron Device Letters (EDL), Future Generation Computing Systems

Teaching & Extracurricular Activities

Georgia Tech: ECE3710 Course — **August 2025 – Present**
Instructor; Prev: Learning Mentor — *Georgia Institute of Technology*

Opportunity Research Scholars (ORS) Program — **August 2025 – Present**
Ph.D. Mentor — *Georgia Institute of Technology*

ECE Graduate Student Association — **August 2024 – Present**
President; Prev: Electrical and Computer Engineering Graduate Representative — *Georgia Institute of Technology*

Graduate Student Government Association — **August 2023 – August 2024**
Academic & Research Affairs Committee Member — *Georgia Institute of Technology*

Beaverton School District — **September 2022 – June 2023**
First Robotics Mentor — *Oregon State University*

EECS Senior Capstone **September 2022 – June 2023**
Project Partner/Mentor *Oregon State University*

IEEE Eta Kappa Nu Honors Society **September 2021 – June 2022**
Member *Oregon State University*

Oregon State Univ. Society of Asian Scientists and Engineers **June 2021 – June 2022**
Treasurer *Oregon State University*

Engineering Student Council **March 2019 – June 2021**
President; Prev: VP of Information & Communication *Oregon State University*