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Ramulator 2.0 Based Hammering Effect Simulation for M3D DRAM

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Laboratory for Emerging Devices and Circuits

Introduction

- Monolithic 3D (M3D) DRAM enables ultra-dense vertical integration, but introduces new **inter-layer RowHammer** and **Floating-Body-Effect (FBE)-amplified Bit Line (BL) hammer** vulnerabilities[1,3,4,5].
- We extend **Ramulator 2.0**[6] with a 3D/subarray-aware controller to accurately model these emerging threats.
- Our model quantifies a **2.75× expanded attack surface** in M3D DRAM compared to traditional 2D designs.
- We further identify efficient mitigation strategies to enable secure, high-density M3D memory design.

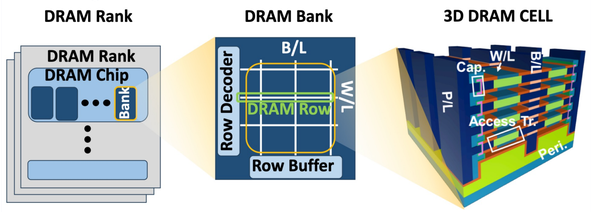


Fig.1: DRAM Organization and Hierarchical Structure from Rank to 3D Cell

Background

M3D DRAM: Stacks layers vertically via BEOL → higher density & lower power vs 2D[2].
RowHammer: Aggressor row activations cause adjacent bit flips. M3D adds vertical inter-layer attacks.
BL Hammer: Frequent bitline toggling triggers bit flips via floating body effect (FBE)[3].

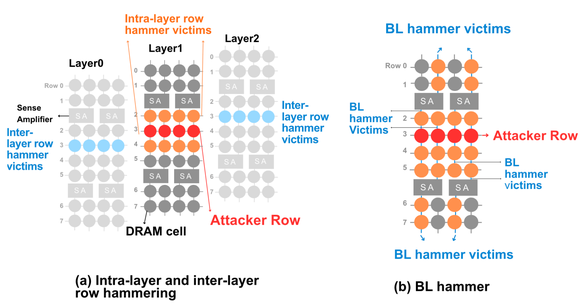


Fig.2: Visualization of (a) Intra-layer and Inter-layer Row Hammer, (b) BL Hammer in M3D DRAM

Implementation

1. 3D Address Decomposition

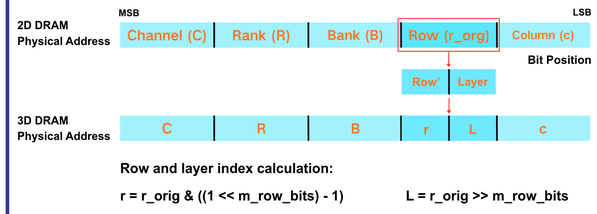
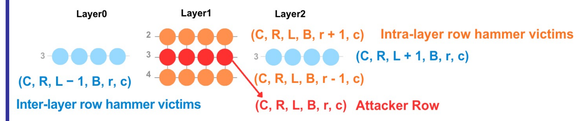


Fig.3: Visualization of Bit Position Partitioning in M3D DRAM Addressing

2. 3D RowHammer Victim Identification



Algorithm 2 3D Victim Identification

Require: Aggressor address (C, R, L, B, r, c)
Ensure: Victim set V

$V \leftarrow \emptyset$
if $r - 1 > 0$ and same subarray **then**
  $V \leftarrow V \cup (C, R, L, B, r-1, c)$
end if
if $r + 1 < maxRow$ and same subarray **then**
  $V \leftarrow V \cup (C, R, L, B, r+1, c)$
end if
Intra-layer RowHammer victims
if $L - 1 > 0$ **then**
  $V \leftarrow V \cup (C, R, L-1, B, r, c)$
end if
if $L + 1 < maxLayer$ **then**
  $V \leftarrow V \cup (C, R, L+1, B, r, c)$
end if
Inter-layer RowHammer victims
if $c - 1 > 0$ **then**
  $V \leftarrow V \cup (C, R, L, B, r, c-1)$
end if
if $c + 1 < maxCol$ **then**
  $V \leftarrow V \cup (C, R, L, B, r, c+1)$
end if
Return V
BL hammer victims

Fig.4: (Top) Visualization of Attacker and Victim Rows in Intra/Inter-Layer RowHammer. **(C, R, L, B, r, c)** specifies the physical location of each DRAM cell in the 3D array.

Fig. 5: (Left) Pseudocode for Constructing Victim Set V from Aggressor Address

3. Time-Window-Based Per-Row Activation Counting and Hammer Detection

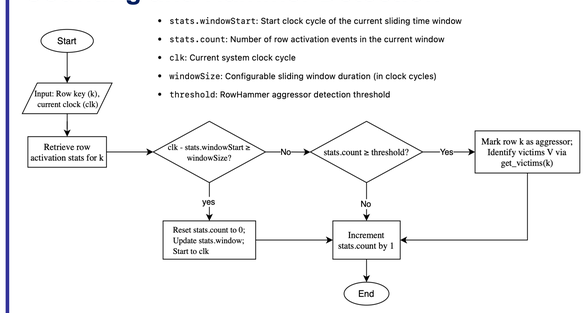


Fig.6: Flowchart of the sliding time window mechanism for RowHammer aggressor detection

Results

- Expanded attack surface in M3D DRAM by **2.75 times** compared to 2D DRAM.

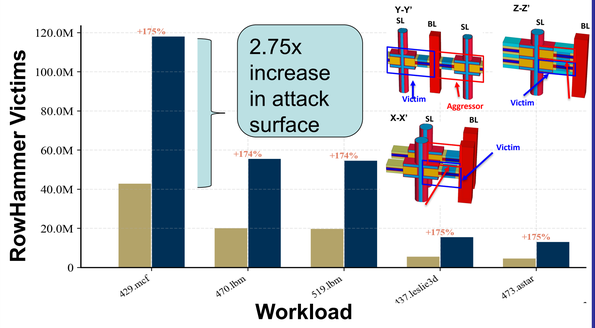


Fig.7: 2D vs. 3D Rowhammer Count

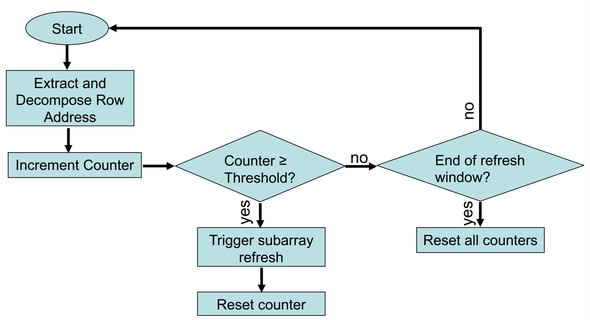


Fig.8: Flowchart of the subarray refresh logic

- Reducing subarray size from 1024 to 128 cells per bitline cuts the mitigation overhead by about 12 times.

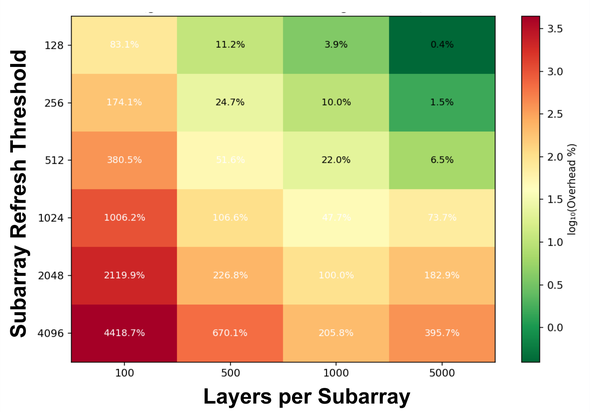


Fig.9: Subarray Refresh Overhead vs Subarray size

Conclusions

- M3D vertical integration expands the RowHammer attack surface by **2.75 times**.
- **Ramulator 2.0** is reusable for evaluating future M3D mitigation proposals.

Future Work

- Investigate the quantitative relationship between e.g., number of stacked layers, subarray size, refresh interval and RowHammer vulnerability.
- Validate M3D Rowhammer characterization with real silicon chips.
- Extend mitigation strategies to composite attacks and optimize the mitigation for system-level deployment in real-world workloads[7].

References

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[7] O. Mutlu, A. Olgun, and A. G. Yaglikci, "Fundamentally understanding and solving RowHammer," in 2023 28th Asia and South Pacific Design Automation Conference (ASP-DAC), 2023.